Chapter 28 The Electrostatic Discharge (ESD) Problem

Consider a chip which is packaged. There must be some lines emanating from the chip to the outside world. If any line is touched by a human being, some static electrical charges will be on this line. These charges may induce a huge voltage which will damage the circuits inside the chip.

In this chapter, we will introduce some mechanisms to neutralize the electrostatic discharge problem.

Section 28.1 A Simple Method to Solve the ESD Problem

Positive Charges

The static charges may be positive or negative. Positive charges will cause a positive high voltage. We first discuss how to solve the positive high voltage problem. To neutralize the high voltage serge, we may use a PMOS transistor which acts as a diode. Consider Fig. 28.1-1

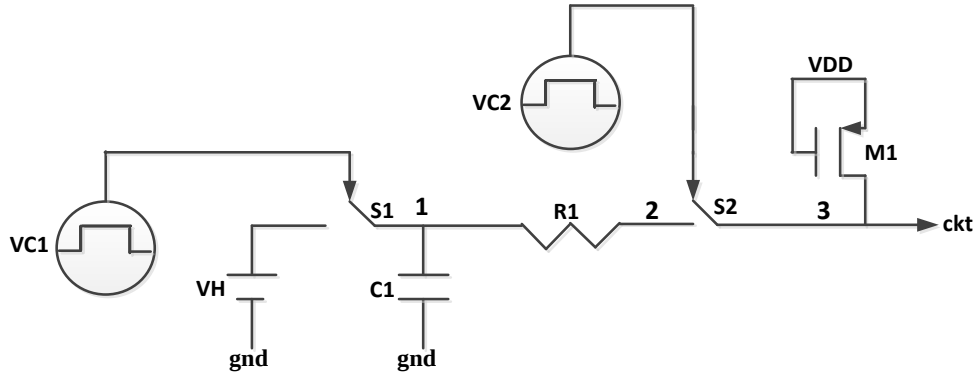


Fig. 28.1-1 Using a PMOS transistor to prevent a positive high positive voltage serge

In Fig. 28.2-1, M2 is a PMOS transistor and M1 is a switch which allows a high voltage to come in. Because the drain of M2 is connected to its gate, it can be considered as a diode as shown in Fig. 28.1-2.

Fig. 28.1-2 The equivalent circuit of M1

VC1 and VC2 are two square waves and there must be a time lag between as shown in Fig. 28.1-3

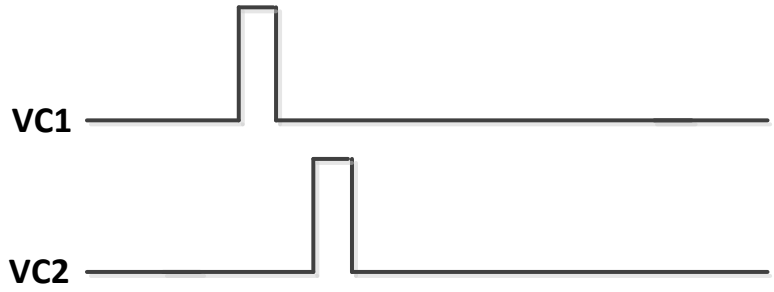


Fig. 28.1-3 VC1 and VC2

The circuit in Fig. 28.1-1 demonstrates the principle of solving the ESD problem. The capacitor C1 represents the place where static electric charges may occur. If there is no static electricity, the voltage of C1 will be low; otherwise it will be high. If this high voltage is transmitted to Node 3. It will be a big disaster. Our job is to prevent this to happen.

VH is a voltage source which represents the static electric charges. If VH is low, it represents the fact that there is not much static electric charges; otherwise, there is a large amount of static electric charges. If VC1 is high, switch S1 is closed, and VH will charge the capacitor. There is a switch S2 controlled by VC2. If VC2 is high, the voltage of C1 will go through S2 to reach Node 3.

If the voltage of C1 is low, there will be no current flowing through M1 and V3 will be low which will not cause any damage to our circuit. If there are a large amount of static electric charges V3 will be temporarily high, but current will flow through M1 . This means that all of the charges will be gone and V3 will go back to normal which is 0.

Experiment 28.1-1 The Circuit in Fig. 28.1-1 When VH is 2V

In this experiment, we test the ESD circuit in Fig. 28.1-1 by assuming VH is 2V. This indicates that there is not much static electric charge. The program is in Table 28.1-1 and the result is in Fig. 28.1-4.

Table 28.1-1 The program for Experiment 28.1-1

```
esd
.protect
.lib “C:\mm0355v.l” TT
.unprotect
.option post
```

```
.op

VDD      VDD      0     3.3V
VSS VSS 0     0V

VH          VH          0           2V
VC1 VC1 0     pulse 0V 3.3V 5u 100n 100n 1u 1000u
VC2 VC2 0     pulse 0V 3.3V 10u 100n 100n 1000u 1000u

G_S1     VH     1    VCR pwl(1)    VC1    0    0,10Meg    3.3v,1m
G_S2     2      3    VCR pwl(1)    VC2    0    0,10Meg    3.3v,1m

C1          1           0           100p
R1          1           2           1.5K

M1   3     VDD      VDD      VDD      PCHW=20U   L=1U

.ic V(1)=0 V(2)=0 V(3)=0
.tran 0.1u 20u
.probe I(M1)
.end
```

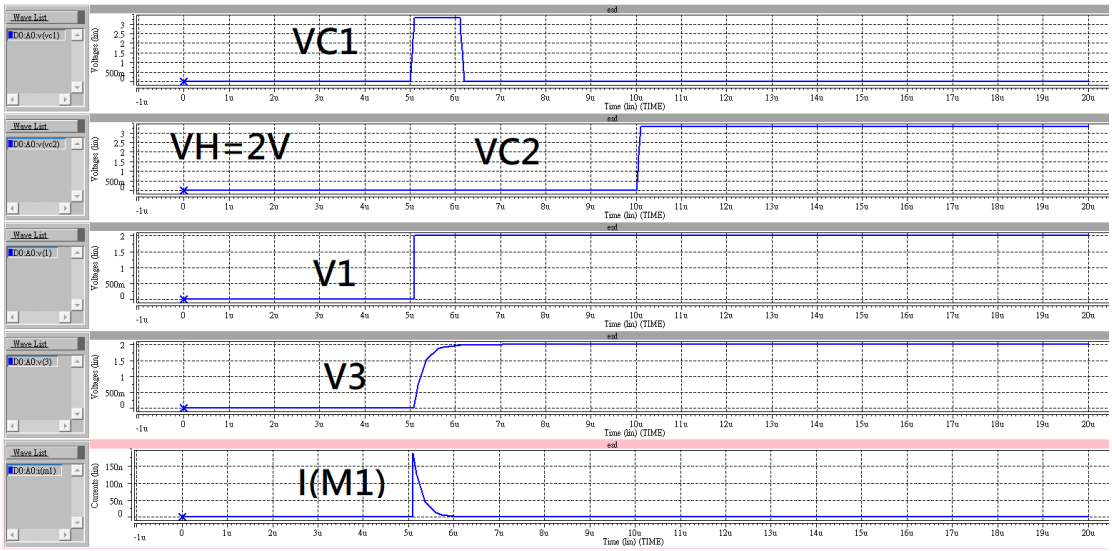


Fig. 28.1-4 The result of Experiment 28.1-1

From Fig. 28.1-4, we can see that VH is transmitted all the way to Node 3 when VH is low. Note that the current in M1 is very small.

Experiment 28.1-2 The Circuit in Fig. 28.1-1 When VH is 1000V

In this experiment, we set VH to be 1000V simulating a a large amount of static electric charges appear. The program is Table 28.1-2 and the result is in Fig. 28.1-5.

Table 28.1-2 The program of Experiment 28.1-2

```
esd
.protect
.lib "C:\mm0355v.l" TT
.unprotect
.option post
.op

VDD VDD 0      3.3V
VSS  VSS  0      0V

VH           VH           0            1000V
VC1  VC1  0      pulse 0V 3.3V 5u 100n 100n 1u 1000u
VC2  VC2  0      pulse 0V 3.3V 10u 100n 100n 1000u 1000u

G_S1      VH      1    VCR pwl(1)    VC1    0    0,10Meg    3.3v,1m
G_S2      2       3    VCR pwl(1)    VC2    0    0,10Meg    3.3v,1m

C1           1            0            100p
R1           1            2            1.5K

M1   3      VDD VDD VDD PCH  W=20U    L=1U

.ic V(1)=0 V(2)=0 V(3)=0
.tran 0.1u 20u
.probe I(M1)
.end
```

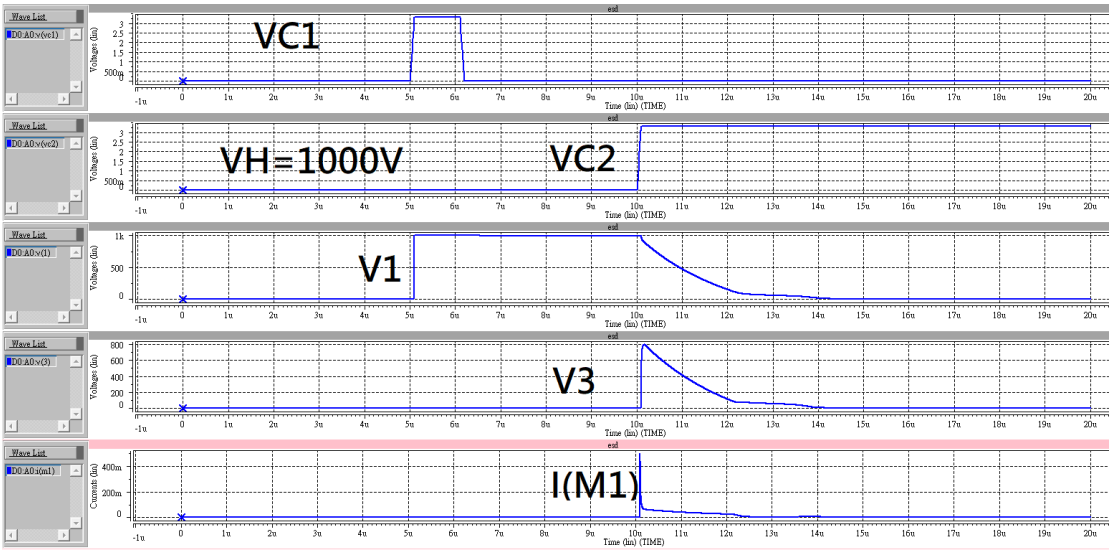


Fig. 28.1-5 The result of Experiment 28.1-2

Fig. 28.1-5 shows that the circuit works because V3 recovers to 0 after V1 becomes extremely high. Note that the current in M1 is very high. This indicates that the static charges disappear as current in M1.

Negative Charges

If the static charges are negative ones, a negative high voltage occurs. In this case, we may use an NMOS transistor to neutralize this voltage. The circuit is as shown in Fig. 28.1-6.

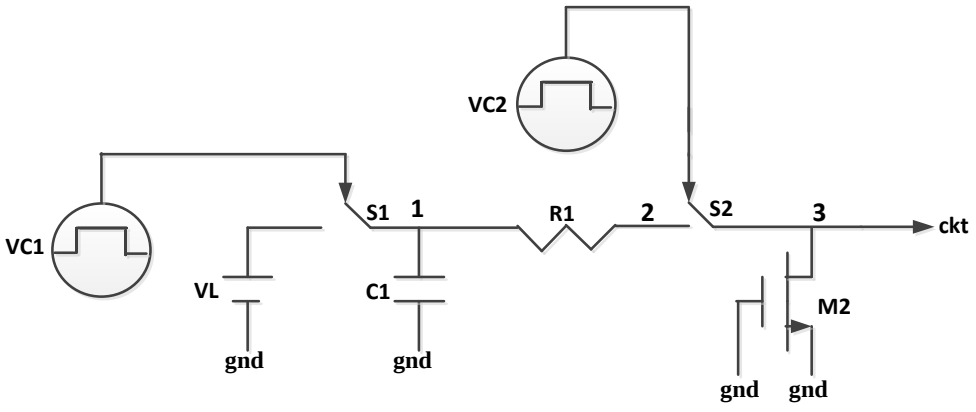


Fig. 28.1-6 Using an NMOS transistor to prevent
a negative high positive voltage serge

Experiment 28.1-3 The Circuit in Fig. 28.1-6 When VL is 2V

In this experiment, we tested the circuit in Fig. 28.1-6 by assuming that VL is 2V. This indicates that there is not much static electric charge. The program is in Table 28.1-3 and the result is in Fig. 28.1-7. As shown in Fig. 28.1-7, V3 reaches 2V and there is almost no current in M2 which is expected.

Table 28.1-3 The program for Experiment 28.1-3

```
Esd
.protect
.lib "C:\mm0355v.l" TT
.unprotect
.option post
.op

VDD VDD 0      3.3V
VSS  VSS  0      0V

VH           VH           0            2V
VC1  VC1  0      pulse 0V 3.3V 5u 100n 100n 1u 1000u
VC2  VC2  0      pulse 0V 3.3V 10u 100n 100n 1000u 1000u

G_S1      VH      1    VCR pwl(1)    VC1    0    0,10Meg    3.3v,1m
G_S2      2       3    VCR pwl(1)    VC2    0    0,10Meg    3.3v,1m

C1           1            0            100p
R1           1            2            1.5K

M2   3      VSS  VSS  VSS  NCH W=20U    L=1U

.ic V(1)=0 V(2)=0 V(3)=0
.tran 0.1u 20u
.probe I(M2)
.end
```

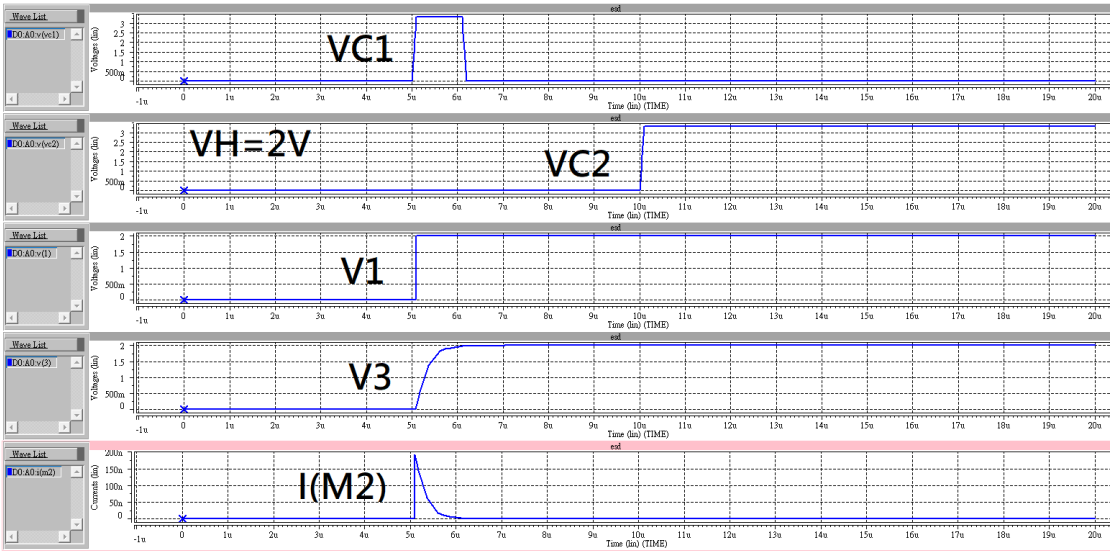


Fig. 28.1-7 The result of Experiment 28.1-3

Experiment 28.1-4 The Circuit in Fig. 28.1-6 When VL is -1000V

In this experiment, we set VL to be -1000V which means that there are a large amount of negative static electric charges. The program is in Table 28.1-4 and the result is in Fig. 28.1-8. As shown in Fig. 28.1-8, V3 goes back to 0V and there is a large current in M2 momentarily which means that the static electric charges have gone through M2 and their effect is neutralized.

Table 28.1-4 The program of Experiment 28.1-4

```
esd
.protect
.lib “C:\mm0355v.l” TT
.unprotect
.option post
.op

VDD VDD 0      3.3V
VSS  VSS  0      0V

VH           VH           0            -1000V
VC1  VC1  0      pulse 0V 3.3V 5u 100n 100n 1u 1000u
VC2  VC2  0      pulse 0V 3.3V 10u 100n 100n 1000u 1000u

G_S1      VH      1    VCR pwl(1)    VC1    0    0,10Meg    3.3v,1m
```

```
G_S2     2      3    VCR pwl(1)    VC2    0    0,10Meg    3.3v,1m

C1          1           0           100p
R1          1           2           1.5K

M2   3      VSS  VSS   VSS   NCH W=20U    L=1U

.ic V(1)=0 V(2)=0 V(3)=0
.tran 0.1u 20u
.probe I(M2)
.end
```

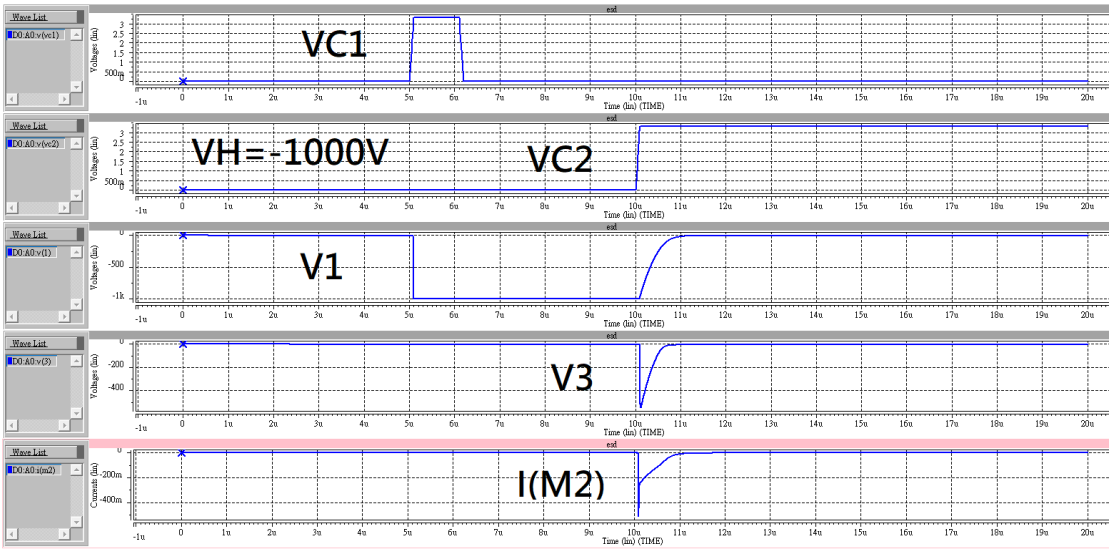


Fig. 28.1-8 The result of Experiment 28.1-4

Complete ESD circuit to Prevent Both Positive and Negative Charges with NMOS and PMOS

To prevent both positive and negative charges, we will use both PMOS and NMOS transistors as shown Fig 28.-9.

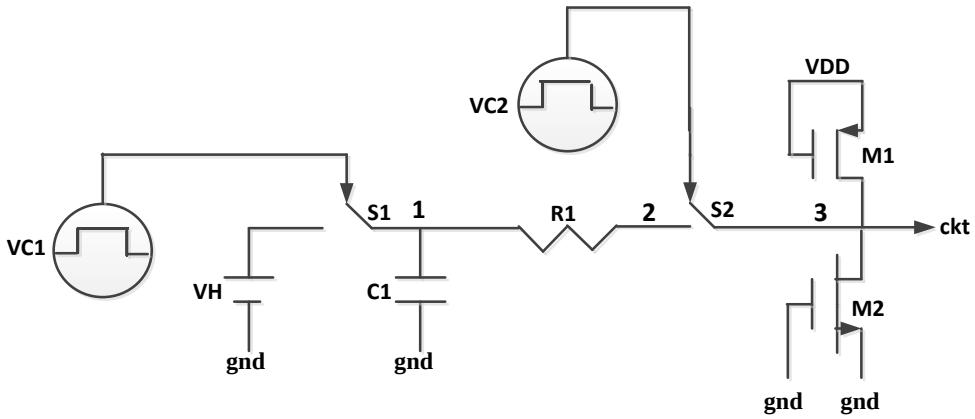


Fig. 28.1-9 An ESD Circuit to Prevent Both Positive and Negative Static Electric Charges.

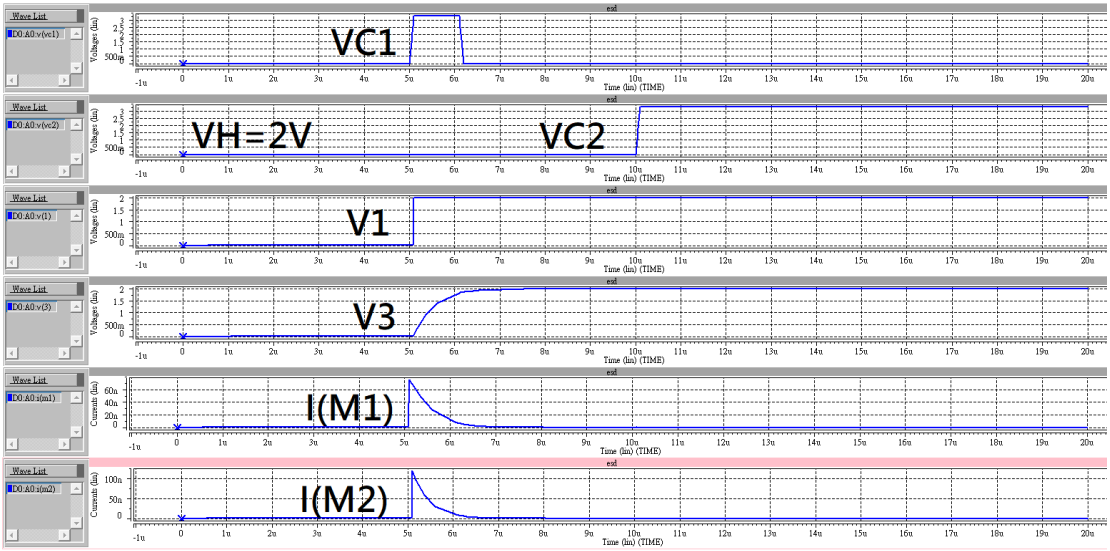
In Fig. 28.1-9, there is a voltage source VH which provides a high positive voltage. This is used for simulating positive static electric charges. If VH is replaced by VL, the circuit can be used to simulate negative static electric charges.

Experiment 28.1-5 The Circuit in Fig. 28.1-9 When VH is 2V

In this experiment, we

```
esd
.protect
.lib "C:\mm0355v.l" TT
.unprotect
.option post
.op

VDD VDD 0      3.3V
VSS  VSS  0      0V

VH           VH           0            2V
VC1  VC1  0      pulse 0V 3.3V 5u 100n 100n 1u 1000u
VC2  VC2  0      pulse 0V 3.3V 10u 100n 100n 1000u 1000u

G_S1      VH      1    VCR pwl(1)    VC1    0    0,10Meg    3.3v,1m
```

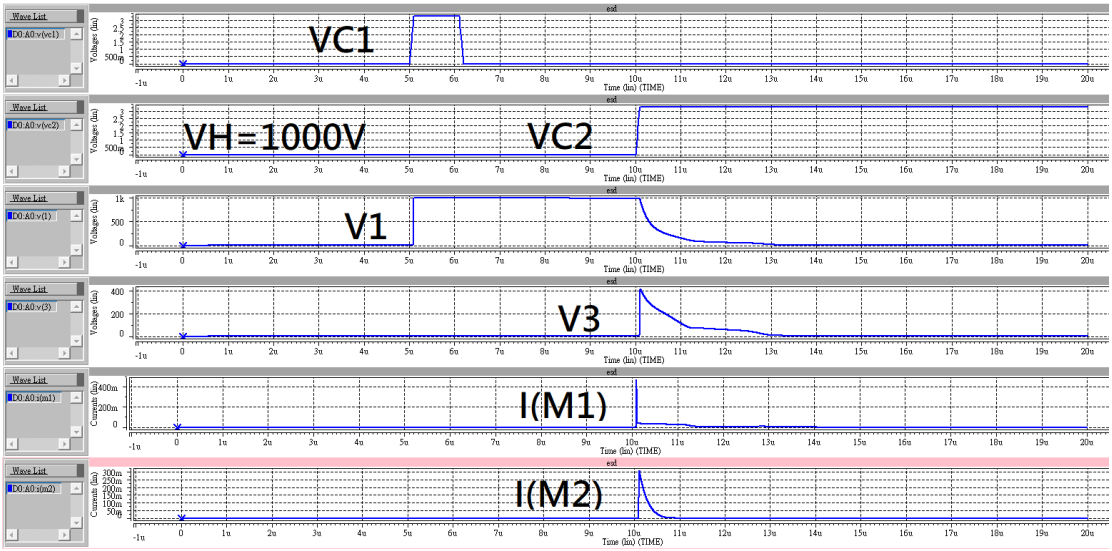
```
G_S2     2      3    VCR pwl(1)    VC2    0    0,10Meg    3.3v,1m

C1          1           0           100p
R1          1           2           1.5K

M1   3      VDD VDD VDD PCH  W=20U    L=1U
M2   3      VSS  VSS  VSS  NCH W=20U    L=1U

.ic V(1)=0 V(2)=0 V(3)=0
.tran 0.1u 20u
.probe I(M1) I(M2)
.end
```



VH=1000V

```
esd
.protect
.lib "C:\mm0355v.l" TT
.unprotect
.option post
.op

VDD VDD 0      3.3V
VSS  VSS  0      0V
```

```
VH          VH          0           1000V
VC1  VC1  0      pulse 0V 3.3V 5u 100n 100n 1u 1000u
VC2  VC2  0      pulse 0V 3.3V 10u 100n 100n 1000u 1000u

G_S1     VH     1    VCR pwl(1)    VC1    0    0,10Meg    3.3v,1m
G_S2     2      3    VCR pwl(1)    VC2    0    0,10Meg    3.3v,1m

C1          1           0           100p
R1          1           2           1.5K

M1   3     VDD VDD VDD PCH  W=20U    L=1U
M2   3     VSS  VSS   VSS   NCH W=20U    L=1U

.ic V(1)=0 V(2)=0 V(3)=0
.tran 0.1u 20u
.probe I(M1) I(M2)
.end
```



VH=-1000V

```
esd
.protect
.lib "C:\mm0355v.l" TT
.unprotect
.option post
```

```
.op

VDD VDD 0      3.3V
VSS  VSS  0      0V

VH           VH           0            -1000V
VC1  VC1  0      pulse 0V 3.3V 5u 100n 100n 1u 1000u
VC2  VC2  0      pulse 0V 3.3V 10u 100n 100n 1000u 1000u

G_S1      VH      1    VCR pwl(1)    VC1    0    0,10Meg    3.3v,1m
G_S2      2       3    VCR pwl(1)    VC2    0    0,10Meg    3.3v,1m

C1           1            0            100p
R1           1            2            1.5K

M1   3      VDD VDD VDD PCH  W=20U    L=1U
M2   3      VSS  VSS  VSS  NCH W=20U    L=1U

.ic V(1)=0 V(2)=0 V(3)=0
.tran 0.1u 20u
.probe I(M1) I(M2)
.end
```